(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2002 (03.01.2002)

PCT

(10) International Publication Number
WO 02/01643 A2

(51) International Patent Classification[7]: H01L 29/00

(21) International Application Number: PCT/US01/19990

(22) International Filing Date: 22 June 2001 (22.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/603,605 26 June 2000 (26.06.2000) US

(71) Applicant *(for all designated States except US)*: **FAIRCHILD SEMICONDUCTOR CORPORATION** [US/US]; 82 Running Hill Road, South Portland, ME 04106 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SHENOY, Praveen, Muraleedharan** [IN/US]; 18 B Wilkeswood Drive, Wilkes-Barre, PA 18702 (US).

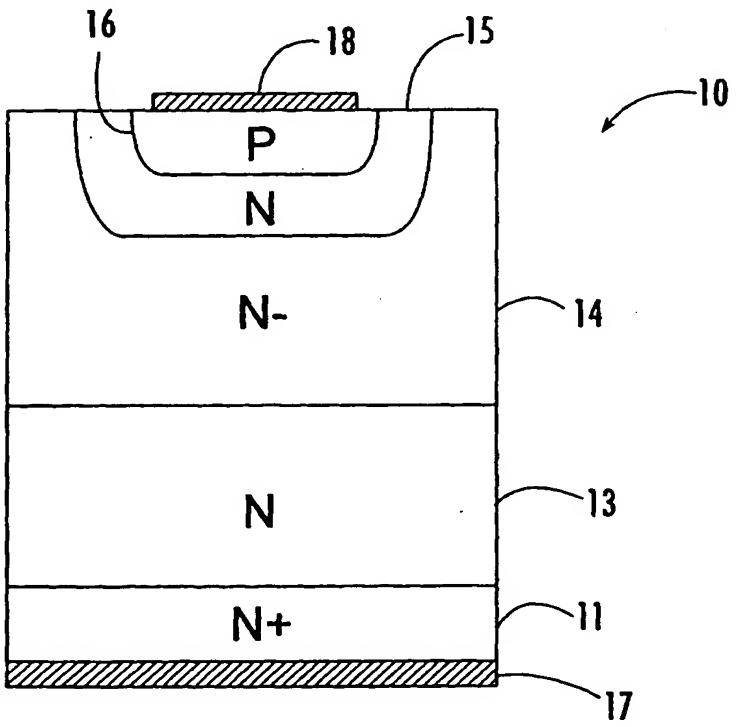
(74) Agents: **REGAN, Christopher, F.** et al.; Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A., 255 South Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, FL 32802-3791 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SOFT RECOVERY POWER DIODE AND RELATED METHOD



(57) Abstract: A semiconductor diode includes a first semiconductor layer including a dopant having a first conductivity type. A second semiconductor layer is adjacent the first semiconductor layer and includes a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of the first semiconductor layer. Adjacent the second semiconductor layer is a third semiconductor layer including a dopant having the first conductivity type and having a dopant concentration greater than the dopant concentration of the second semiconductor layer. A fourth semiconductor layer is adjacent the third semiconductor layer and includes a dopant of a second conductivity type. Respective contacts are connected to the first and fourth semiconductor layers.

WO 02/01643 A2

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SOFT RECOVERY POWER DIODE AND RELATED METHOD

Field of the Invention

The present invention relates to the field of electronic devices, and, more particularly, to power diodes.

Background of the Invention

Diodes are used in a variety of circuits to either restrict or permit the flow of current within the circuit depending upon the voltage which is applied across the diode. That is, the voltage will either cause the diode to become forward-biased, at which point the current will flow through the diode, or reverse-biased, at which point current is restricted from flowing through the diode.

Diodes such as the P-i-N (positive-intrinsic-negative) diodes are widely used in high voltage applications, such as power factor correction circuits, for example. When such a diode transitions suddenly from a forward-biased state to a reversed-biased state caused by a large voltage swing, the diode must undergo a period of reverse recovery. During the forward-biased state the i region of the diode contains a large concentration of minority carriers. This concentration must be removed from the i region before the current flow can be limited to substantially zero.

Accordingly, after being switched to a reverse-biased state a reverse recovery current (Irr) will increase in magnitude until the excess carrier concentration at the P-N junction has dropped below the background concentration at a time t (i.e., the time when the current reaches a negative peak), at which point reverse recovery can begin.

If the minority carrier concentration becomes too large, it is possible that the Irr may increase to the point at which the circuit is damaged. Accordingly, it is desirable to have a low Irr to avoid this disadvantage. Yet, reducing the Irr results in an increase in the forward voltage drop (Vf) of the diode as well a decrease in the softness of the recovery waveform, both of which are undesirable. The softness of the recovery waveform corresponds to the slope of the Irr (i.e., dIrr/dt) as it tends toward zero after the time t. The steeper the slope, the less "soft" the recovery waveform and the greater the chance that ringing will result. Ringing is caused when the current overshoots or oscillates back and forth about zero during the reverse recovery period because the current increases and decreases too quickly due to circuit parasitics.

Accordingly, there is a need for a power diode that provides for a relatively low Irr value while maintaining a low Vf and soft recovery characteristics. Various attempts have been made in the prior art to create such diodes. One example is U.S. Patent No. 4,594,602 to Iimura et al. entitled "High Speed Diode." The diode has a PNN<+> structure which is intended to provide high speed switching characteristics along with a soft reverse recovery and low forward voltage drop. However, the structure of this diode may not provide an adequate balance of

reduced Irr and increased softness in certain applications.

Summary of the Invention

In view of the foregoing background, it is therefore an object of the invention to provide a semiconductor diode having relatively low Irr and Vf values and further exhibiting soft recovery characteristics.

This and other objects, features, and advantages in accordance with the present invention are provided by a semiconductor diode including a more highly doped base layer between the intrinsic layer and the base. More particularly, the diode may comprise a first semiconductor layer that includes a dopant having a first conductivity type and a second semiconductor layer adjacent the first semiconductor layer that includes a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of the first semiconductor layer. Additionally, a third semiconductor layer maybe adjacent the second semiconductor layer and includes a dopant having the first conductivity type and having a dopant concentration greater than the dopant concentration of the second semiconductor layer. This third layer may be considered as providing the more highly doped base layer or region. A fourth semiconductor layer maybe adjacent the third semiconductor layer and include a dopant of a second conductivity type. Respective contacts are connected to the first and fourth semiconductor layers. The diode has a reduced Irr compared to prior art diodes yet still provides a low Vf and soft recovery characteristics.

The semiconductor diode may further include an intermediate semiconductor layer between the first

semiconductor layer and the second semiconductor layer. The intermediate semiconductor layer has a dopant concentration between the dopant concentrations of the first and second semiconductor layers. Additionally, the fourth semiconductor layer may be surrounded by the third semiconductor layer.

By way of example, the dopant concentrations and thicknesses of the semiconductor layers may be as follows: for the first semiconductor layer, a dopant concentration in a range of about 1 X 10^{18} to 1 X 10^{19} cm^{-3} and a thickness in a range of about 100 to 400 μm; for the intermediate semiconductor layer, a dopant concentration in a range of about 2.5 x 10^{14} to 1.3 x 10^{15} cm^{-3} and a thickness in a range of about 8 to 35 μm; for the second semiconductor layer, a dopant concentration in a range of about 6 x 10^{13} to 6 x 14^{14} cm^{-3} and a thickness in a range of about 7 to 70 μm; for the third semiconductor layer, a dopant concentration in a range of about 1 X 10^{14} to 1 X 10^{16} cm^{-3} and a thickness in a range of about 4 to 6 μm; and for the fourth semiconductor layer, a dopant concentration in a range of less than about 1 X 10^{17} cm^{-3} and a thickness in a range of about 2 to 4 μm.

In addition, the first conductivity type is preferably N type and the second conductivity type is preferably P type. Another aspect of the invention relates to doping the fourth semiconductor region with relatively low concentrations compared to those found in prior art devices. Accordingly, the excess carrier concentration at the P-N junction between the third and fourth semiconductor layers is held to a lower level, thus resulting in a reduced Irr at the time t (hereafter "Irrm"). Increasing the doping concentration of the third semiconductor layer further reduces the carrier concentration at the P-N junction,

providing for further reduction in the Irrm. The dopant concentration of the fourth semiconductor layer preferably has a dopant concentration greater than the dopant concentration of the third semiconductor layer. Furthermore, the dopant concentration may be chosen to cause an excess carrier concentration region away from the P-N junction during operation to be higher than in prior art devices, which serves to maintain Vf at low values and produce a soft recovery waveform.

A method according to the invention is for making a semiconductor diode. The method preferably includes providing a semiconductor substrate including a dopant having a first conductivity type. A first epitaxial layer of the first conductivity type is grown adjacent the semiconductor substrate and may have a dopant concentration less than a dopant concentration of the first semiconductor layer. The method may further include doping a first region of the first conductivity type in the first epitaxial layer to a dopant concentration less than the dopant concentration of the first epitaxial layer, and doping a second region of a second conductivity type in the first region. Additionally, respective contacts maybe formed on the semiconductor substrate and the second region.

Brief Description of the Drawings

FIG. 1 is a schematic cross-sectional view of a semiconductor diode according to the present invention.

FIG. 2 is a graph illustrating a doping profile of the semiconductor diode of FIG. 1.

FIG. 3 is a graph illustrating simulated test results of the recovery waveforms of a prior art diode and several embodiments of diodes according to the present invention.

FIG. 4 is a graph illustrating actual test results of the recovery waveforms of a prior art diode and a diode according to the present invention.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring now to FIG. 1, a diode **10** according to the invention is first described. The diode **10** includes a first semiconductor layer or substrate **11** that illustratively includes an N-type dopant. An intermediate semiconductor layer **13** (N-type) is formed between the first semiconductor layer **11** and a second semiconductor layer **14**, which is also N-type. The dopant concentration of the intermediate semiconductor layer **13** is less than that of first semiconductor layer **11**, and the dopant concentration of the second semiconductor layer **14** is less than that of the intermediate semiconductor layer. The intermediate and second semiconductor layers **13, 14** may be epitaxially grown on the substrate, for example, as will be readily appreciated by those skilled in the art.

A third semiconductor layer **15** is adjacent the second semiconductor layer **14** and includes an N-type dopant of a concentration greater than the second semiconductor layer. Adjacent the third semiconductor

layer is a fourth semiconductor layer **16** which includes a P-type dopant. Both the third and fourth semiconductor layers **15, 16** may be doped by conventional diffusion or implantation techniques, for example, as will be readily appreciated by those of skill in the art. As shown in FIG. 1, the fourth semiconductor layer **16** may be surrounded by the third semiconductor layer **15**. A metal contact layer (or cathode) **17** is formed on the first semiconductor layer **11** and a metal contact layer (or anode) **18** is formed on the fourth semiconductor layer **16**. A shallow, lightly activated P+ surface implant may be included to provide better contact between the fourth semiconductor layer **16** and the anode **18**. The implant layer is only lightly activated to keep the injection efficiency at the P-N junction low.

According to the present invention, the dopant concentrations of the above layers are chosen to minimize carrier concentration around the P-N junction between the third and fourth semiconductor layers **15, 16** to thereby lower Irrm. This can be achieved in two ways. First, the doping concentration of the third semiconductor layer **15** may be higher than the doping concentration of the second layer **14**. Secondly, the doping concentration of the fourth semiconductor layer **16** may be decreased relative to prior art devices, providing the same effect. That is, by reducing the injection efficiency of the P type injector the excess carrier concentration at the P-N junction may be lowered. By doing both, an even greater reduction in Irrm levels may be obtained, as will be discussed further below.

As noted above, reducing Irrm normally leads to an increase in Vf and a loss of softness in the

recovery waveform. To alleviate such results, the dopant concentrations are chosen to cause an excess carrier concentration region to be formed away from the P-N junction during operation, which serves to maintain Vf at low values and produce a soft recovery waveform. That is, even though the maximum recovery value (i.e., the point at which dIrr/dt equals zero) is reduced because a lower carrier concentration is present at the P-N junction, the overall carrier concentration of the semiconductor diode **10** may be maintained due to the higher excess carrier concentration region away from the P-N junction, which allows Vf to remain low. Also, since the maximum recovery value is lower, the time it takes the reverse recovery current to reach this point will decrease. Yet, since the carrier concentration across the entire semiconductor diode **10** remains substantially the same as in prior art diodes, the total time required for recovery will basically remain unchanged. Thus, the slope of the recovery curve after the maximum recovery value (i.e., after time t) will be less steep, resulting in increased softness.

Exemplary expected ranges for the thicknesses (in μm) and doping concentrations (in cm^{-3}) of the above described layers for representative diodes of 300, 600, and 1200 volts are provided in Table 1 and Table 2, respectively, below. Those of skill in the art will appreciate that the above advantages may be implemented in a variety of diodes having a variety of operating voltages other than those provided in these tables. Layer numbers refer to the reference numeral given above for the respective layer.

Table 1 - Thicknesses

Layer	300V	600V	1200V
11	100 - 400 μm	100 - 400 μm	100 - 400 μm
13	8 - 10 μm	25 - 30 μm	30 - 35 μm
14	7 - 9 μm	25 - 30 μm	60 - 70 μm
15	4 - 6 μm	4 - 6 μm	4 - 6 μm
16	2 - 4 μm	2 - 4 μm	2 - 4 μm

Table 2 - Doping Concentrations

Layer	300V	600V	1200V
11	1×10^{18} - 1×10^{19} cm^{-3}	1×10^{18} - 1×10^{19} cm^{-3}	1×10^{18} - 1×10^{19} cm^{-3}
13	1×10^{15} - 1.3×10^{15} cm^{-3}	5×10^{14} - 7×10^{14} cm^{-3}	2.5×10^{14} - 3×10^{14} cm^{-3}
14	5×10^{14} - 6×10^{14} cm^{-3}	1×10^{14} - 1.2×10^{14} cm^{-3}	6×10^{13} - 7×10^{13} cm^{-3}
15	1×10^{15} - 1×10^{16} cm^{-3}	2×10^{14} - 4×10^{15} cm^{-3}	1×10^{14} - 3×10^{15} cm^{-3}
16	$< 1 \times 10^{17}$ cm^{-3}	$< 1 \times 10^{17}$ cm^{-3}	$< 1 \times 10^{17}$ cm^{-3}

An exemplary dopant profile of the semiconductor diode **10** of FIG. 1 is shown in FIG. 2. The reference numbers again correspond to the above described layers. One noteworthy point illustrated by the profile is that the dopant concentration of the fourth semiconductor layer **16** is chosen to be greater than the dopant concentration of the third semiconductor layer **15**. Additionally, the depth of the fourth semiconductor layer **16** is less than corresponding P-layers of prior art P-N diodes, which are typically about 8μm. Furthermore, the dopant concentration of the fourth semiconductor layer **16** is

also less than that of prior art diodes, as will be appreciated by those of skill in the art. Accordingly, the total charge of the semiconductor layer **16** is reduced to thereby provide a lower injection efficiency at the P-N junction than in prior art diodes.

The efficacy of the present invention has been demonstrated in both simulations and actual tests. Turning now to FIG. 3, the simulated recovery waveforms of four different 600V diodes are illustrated. The first waveform **20** corresponds to a prior art Hyperfast diode made by the assignee of the present invention. The second waveform **21** corresponds to a diode made according to the present invention having a third semiconductor layer **15** with an increased dopant concentration (as described in Table 2, above) and a conventionally doped fourth semiconductor layer **16**. The third waveform **22** corresponds to a diode made according to the present invention having a fourth semiconductor layer **16** with a decreased dopant concentration (again described in Table 2) and a conventionally doped third semiconductor layer **15**. Finally, the fourth waveform **23** corresponds to a diode made according to the present invention having both a third semiconductor layer **15** with an increased dopant concentration and a fourth semiconductor layer **16** with a decreased dopant concentration.

Each of the simulated diodes according to the present invention (i.e., waveforms **21, 22, 23**) provide lower Irr values and increased softness. Specifically, the Irr of the diodes corresponding to waveforms **21, 22** were approximately 9 and 14% lower, respectively, than the Irr of the prior art diode corresponding to waveform **20**. Furthermore, the diode corresponding to waveform **23** provided an approximate 27% drop in Irr as

well as an approximate 75% increase in softness with respect to the prior art diode. These values were obtained while maintaining Vf at about 1.8 ± 0.05 volts for each of the diodes.

Referring now to FIG. 4, actual test results comparing the above prior art Hyperfast diode to a diode according to the invention having both a third semiconductor layer **15** with an increased dopant concentration and a fourth semiconductor layer **16** with a decreased dopant concentration are shown. The waveform **24** corresponds to the prior art diode and the waveform **25** corresponds to the diode of the present invention. Again, it can be seen that the Irr for the diode of the present invention is lower than that of the prior art diode (by approximately 26%). Most notably, an increase in softness of approximately 130% was realized, resulting in substantially no ringing. Again, by selecting dopant concentrations sufficient to cause an excess carrier concentration region as described above, the Vf value of the diode according to the present invention was maintained substantially the same as that of the prior art diode.

As will be appreciated by those skilled in the art, the third and fourth semiconductor layer **15**, **16** of the diode **10**, can be formed as doped regions in the upper portion of the second semiconductor layer **14**. This can be done by conventional implantation or other doping techniques as will be appreciated by those skilled in the art. Accordingly, the power semiconductor diode **10** with its advantageous features can be readily made using an additional selective doping step to form the third semiconductor layer **15** (first doped region) as will be readily appreciated by those skilled in the art.

A method according to the invention is for making the semiconductor diode **10** and may include providing a doped semiconductor substrate **11** and growing epitaxial layers **13, 14** on the semiconductor substrate. The third layer or first region **15** is formed by doping an upper portion of the epitaxial layer **14**, and the second region **16** may be formed by doping an upper portion of the first region. The contacts **17, 18** are also preferably formed on the semiconductor substrate **11** and the second region **16**, respectively, as will be readily appreciated by those skilled in the art. The above layers are preferably formed having the dopant types and concentrations, thickness, etc. as set forth above.

It will also be appreciated by those skilled in the art that the present invention is not limited to any one type of diode. Rather, it may advantageously be used in all diodes including a P-N junction where a soft Irr waveform is desired, such as MOSFET body diodes, for example.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that other modifications and embodiments are intended to be included within the scope of the appended claims.

THAT WHICH IS CLAIMED IS:

1. A semiconductor diode comprising:

a first semiconductor layer including a dopant having a first conductivity type;

a second semiconductor layer adjacent said first semiconductor layer and including a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of said first semiconductor layer;

a third semiconductor layer adjacent said second semiconductor layer and including a dopant having the first conductivity type and having a dopant concentration greater than the dopant concentration of said second semiconductor layer;

a fourth semiconductor layer adjacent said third semiconductor layer and including a dopant of a second conductivity type; and

respective contacts connected to said first and fourth semiconductor layers.

2. The semiconductor diode of Claim 1 wherein said fourth semiconductor layer has a dopant concentration greater than the dopant concentration of said third semiconductor layer.

3. The semiconductor diode of Claim 1 wherein said third semiconductor layer has a thickness in a range of about 4 to 6 μm.

4. The semiconductor diode of Claim 1 wherein the dopant concentration of said third semiconductor layer is in a range of about 1×10^{14} to 1×10^{16} cm^{-3}.

5. The semiconductor diode of Claim 1 wherein said fourth semiconductor layer has a thickness of about 2 to 4 μm.

6. The semiconductor diode of Claim 1 wherein said fourth semiconductor layer has a dopant concentration in a range of less than about 1×10^{17} cm^{-3}.

7. The semiconductor diode of Claim 1 wherein said fourth semiconductor layer is surrounded by said third semiconductor layer.

8. The semiconductor diode of Claim 1 wherein said first semiconductor layer has a thickness in a range of about 100 to 400 μm.

9. The semiconductor diode of Claim 1 wherein the dopant concentration of said first semiconductor layer is in a range of about 1×10^{18} to 1×10^{19} cm^{-3}.

10. The semiconductor diode of Claim 1 wherein said second semiconductor layer has a thickness in a range of about 7 to 70 μm.

11. The semiconductor diode of Claim 1 wherein the dopant concentration of said second semiconductor layer is in a range of about 6×10^{13} to 6×10^{14} cm^{-3}.

12. The semiconductor diode of Claim 1 further comprising an intermediate semiconductor layer between said first semiconductor layer and said second semiconductor layer including a dopant having the first conductivity type and having a dopant concentration between the dopant concentration of said first semiconductor layer and the dopant concentration of said second semiconductor layer.

13. The semiconductor diode of Claim 12 wherein said intermediate semiconductor layer has a thickness in a range of about 8 to 35 μm.

14. The semiconductor diode of Claim 12 wherein the dopant concentration of said intermediate

semiconductor layer is in a range of about 2.5×10^{14} to 1.3×10^{15} cm^{-3}.

15. The semiconductor diode of Claim 1 wherein the first conductivity type is N type and the second conductivity type is P type.

16. A semiconductor diode comprising:

a first semiconductor layer including a dopant having a first conductivity type;

a second semiconductor layer adjacent said first semiconductor layer and including a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of said first semiconductor layer;

a first doped region in said second semiconductor layer having the first conductivity type and having a dopant concentration greater than the dopant concentration of said second semiconductor layer;

a second doped region in said first doped region having a second conductivity type; and

respective contacts connected to said first semiconductor layer and said second doped region.

17. The semiconductor diode of Claim 16 wherein said second doped region has a dopant concentration greater than the dopant concentration of said first doped region.

18. The semiconductor diode of Claim 16 wherein said first doped region has a thickness in a range of about 4 to 6 μm.

19. The semiconductor diode of Claim 16 wherein the dopant concentration of said first doped region is in a range of about 1×10^{14} to 1×10^{16} cm^{-3}.

20. The semiconductor diode of Claim 16 wherein said second doped region has a thickness of about 2 to 4 μm.

21. The semiconductor diode of Claim 16 wherein said second doped region has a dopant concentration in a range of less than about 1×10^{17} cm^{-3}.

22. The semiconductor diode of Claim 16 wherein said second doped region is surrounded by said first doped region.

23. The semiconductor diode of Claim 16 wherein said first semiconductor layer has a thickness in a range of about 100 to 400 μm.

24. The semiconductor diode of Claim 16 wherein the dopant concentration of said first semiconductor layer is in a range of about 1×10^{18} to 1×10^{19} cm^{-3}.

25. The semiconductor diode of Claim 16 wherein said second semiconductor layer has a thickness in a range of about 7 to 70 μm.

26. The semiconductor diode of Claim 16 wherein the dopant concentration of said second semiconductor layer is in a range of about 6×10^{13} to 6×10^{14} cm^{-3}.

27. The semiconductor diode of Claim 16 further comprising an intermediate semiconductor layer between said first semiconductor layer and said second semiconductor layer including a dopant having the first conductivity type and having a dopant concentration between the dopant concentration of said first semiconductor layer and the dopant concentration of said second semiconductor layer.

28. The semiconductor diode of Claim 27 wherein said intermediate semiconductor layer has a thickness in a range of about 8 to 35 μm.

29. The semiconductor diode of Claim 27 wherein the dopant concentration of said intermediate semiconductor layer is in a range of about 2.5×10^{14} to 1.3×10^{15} cm^{-3}.

30. The semiconductor diode of Claim 16 wherein the first conductivity type is N type and the second conductivity type is P type.

31. A semiconductor diode comprising:

a first semiconductor layer including a dopant having a first conductivity type;

a second semiconductor layer adjacent said first semiconductor layer and including a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of said first semiconductor layer;

a first doped region in said second semiconductor layer having the first conductivity type and having a dopant concentration greater than the dopant concentration of said second semiconductor layer;

a second doped region in said first doped region having a second conductivity type and having a dopant concentration greater than the dopant concentration of said first doped region; and

respective contacts connected to said first semiconductor layer and said second doped region.

32. The semiconductor diode of Claim 31 wherein said first doped region has a thickness in a range of about 4 to 6 μm.

33. The semiconductor diode of Claim 31 wherein the dopant concentration of said first doped region is in a range of about 1×10^{14} to 1×10^{16} cm^{-3}.

34. The semiconductor diode of Claim 31 wherein said second doped region has a thickness of about 2 to 4 μm.

35. The semiconductor diode of Claim 31 wherein said second doped region has a dopant concentration in a range of about to 1 x 10^{17} cm^{-3}.

36. The semiconductor diode of Claim 31 wherein said second doped region is surrounded by said first doped region.

37. The semiconductor diode of Claim 31 wherein said first semiconductor layer has a thickness in a range of about 100 to 400 μm.

38. The semiconductor diode of Claim 31 wherein the dopant concentration of said first semiconductor layer is in a range of about 1 X 10^{18} to 1 x 10^{19} cm^{-3}.

39. The semiconductor diode of Claim 31 wherein said second semiconductor layer has a thickness in a range of about 7 to 70 μm.

40. The semiconductor diode of Claim 31 wherein the dopant concentration of said second semiconductor layer is in a range of about 6 x 10^{13} to 6 x 10^{14} cm^{-3}.

41. The semiconductor diode of Claim 31 further comprising an intermediate semiconductor layer between said first semiconductor layer and said second semiconductor layer including a dopant having the first conductivity type and having a dopant concentration between the dopant concentration of said first semiconductor layer and the dopant concentration of said second semiconductor layer.

42. The semiconductor diode of Claim 41 wherein said intermediate semiconductor layer has a thickness in a range of about 8 to 35 μm.

43. The semiconductor diode of Claim 41 wherein the dopant concentration of said intermediate semiconductor layer is in a range of about 2.5×10^{14} to 1.3×10^{15} cm^{-3}.

44. The semiconductor diode of Claim 31 wherein the first conductivity type is N type and the second conductivity type is P type.

45. A method for making a semiconductor diode comprising:

providing a semiconductor substrate including a dopant having a first conductivity type;

growing a first epitaxial layer of the first conductivity type adjacent the semiconductor substrate and having a dopant concentration less than a dopant concentration of the semiconductor substrate;

doping a first region of the first conductivity type in the first epitaxial layer to a dopant concentration greater than the dopant concentration of the first epitaxial layer;

doping a second region of a second conductivity type in the first region; and

forming respective contacts on the semiconductor substrate and the second region.

46. The method of Claim 45 wherein doping the second region comprises doping the second region to a greater dopant concentration than the dopant concentration of the first region.

47. The method of Claim 45 wherein doping the first region comprises doping the first region to a depth in a range of about 4 to 6 μm.

48. The method of Claim 45 doping the first region comprises doping the first region to a dopant concentration in a range of about 1×10^{14} to 1×10^{16} cm^{-3}.

49. The method of Claim 45 wherein doping the second region comprises doping the second region to a depth in a range of about 2 to 4 μm.

50. The method of Claim 45 wherein doping the second region comprises doping the second region to a dopant concentration in a range of less than about 1×10^{17} cm^{-3}.

51. The method of Claim 45 further comprising growing a second epitaxial layer of the first conductivity type between the semiconductor substrate and the first epitaxial layer and having a dopant concentration between the dopant concentration of the semiconductor substrate and the dopant concentration of the first epitaxial layer.

52. The method of Claim 45 wherein the first conductivity type is N type and the second conductivity type is P type.

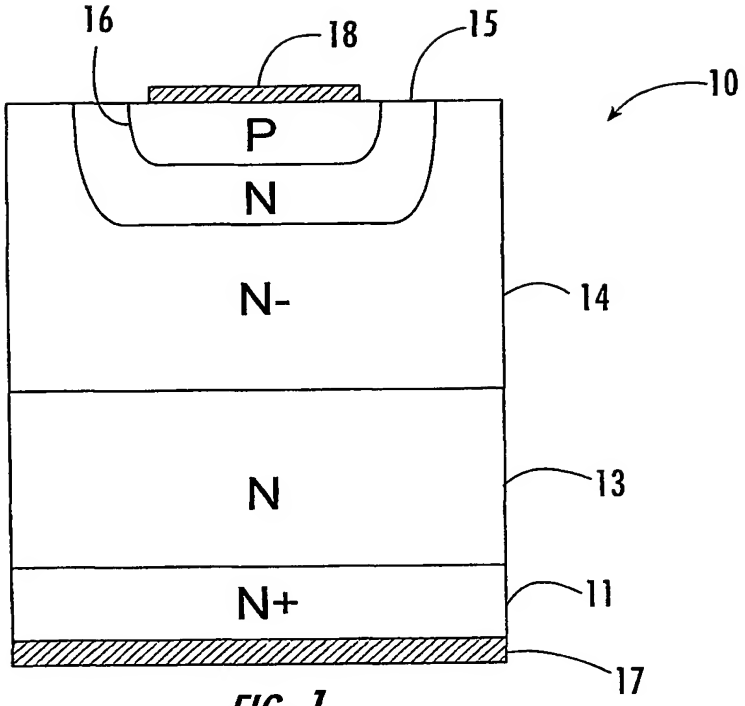


FIG. 1.

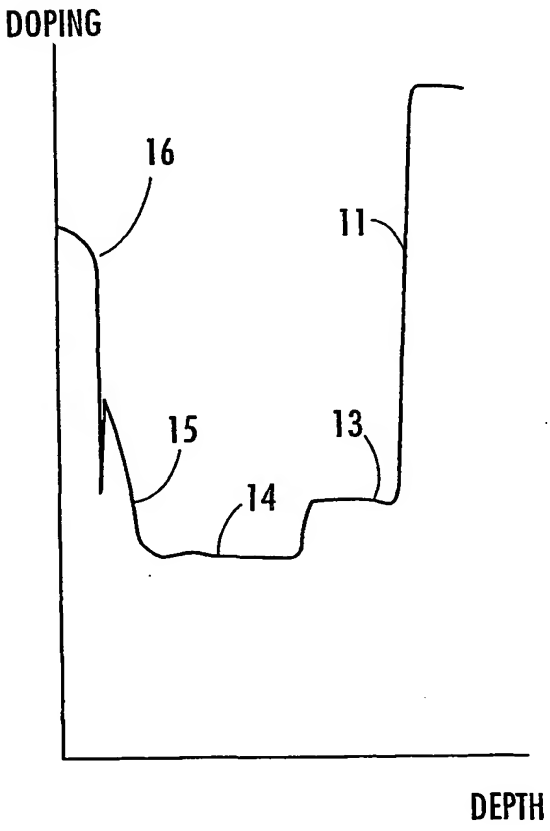


FIG. 2.

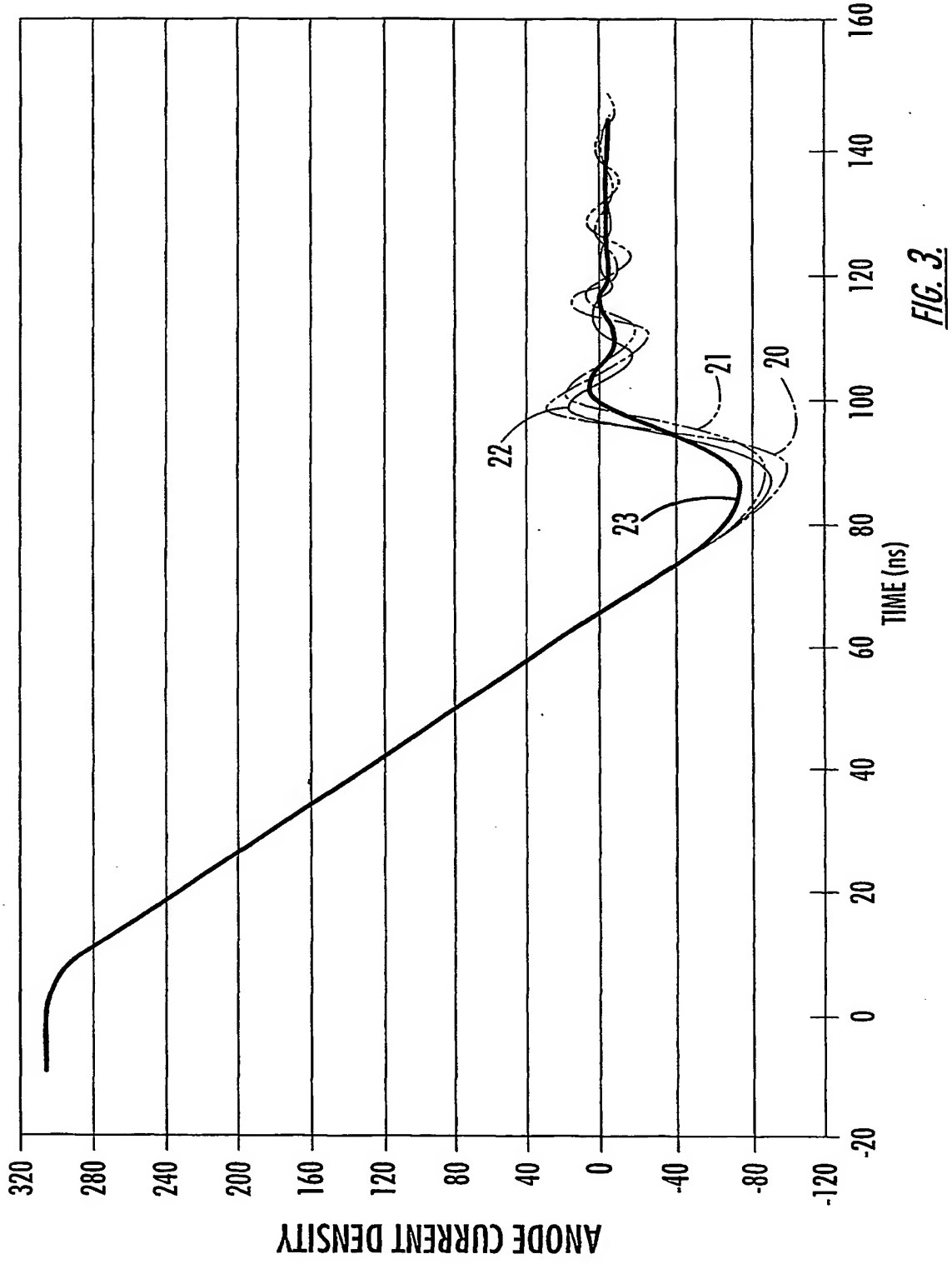


FIG. 3.

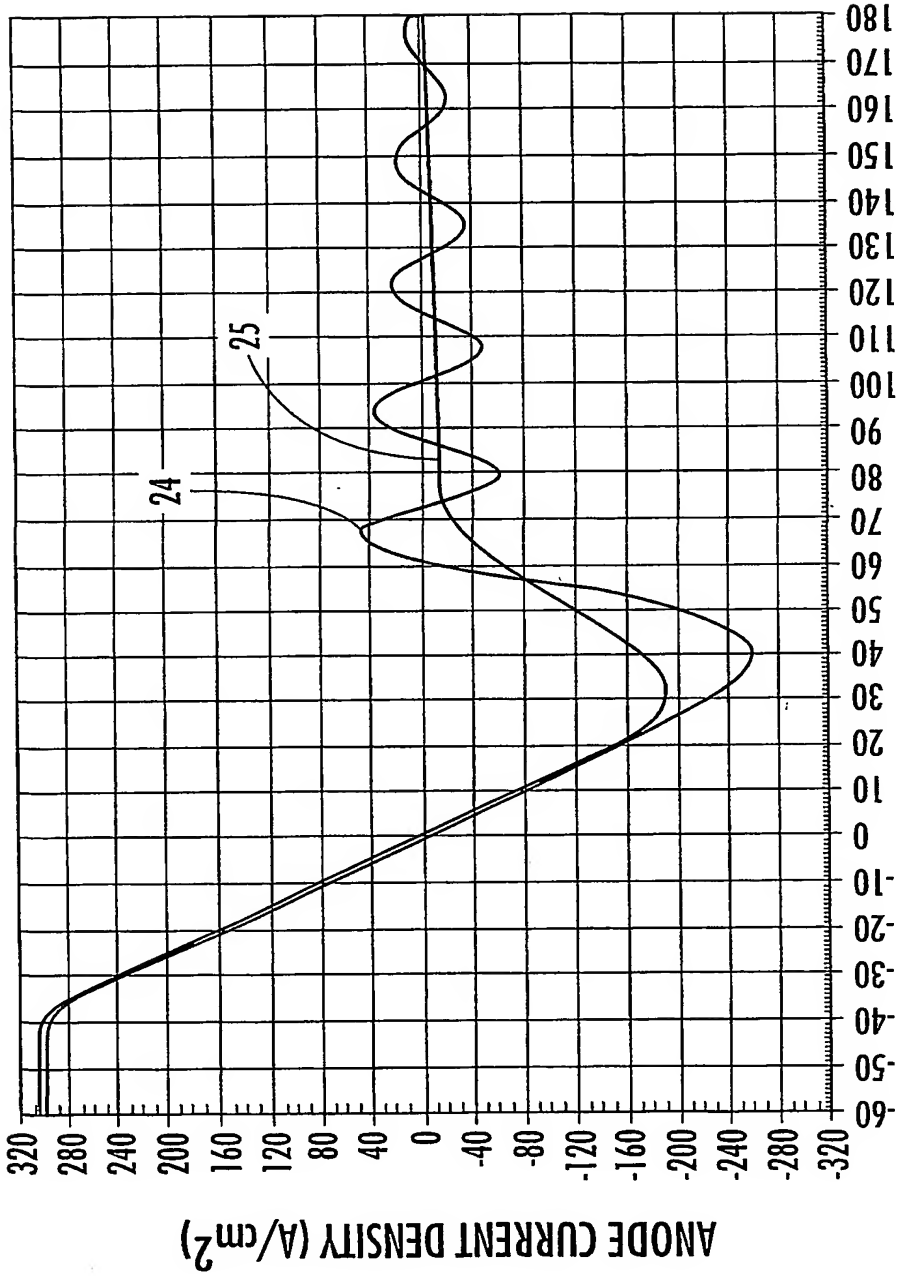


FIG. 4.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2002 (03.01.2002)

PCT

(10) International Publication Number
WO 02/01643 A3

(51) International Patent Classification[7]: H01L 29/861

(21) International Application Number: PCT/US01/19990

(22) International Filing Date: 22 June 2001 (22.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/603,605 26 June 2000 (26.06.2000) US

(71) Applicant *(for all designated States except US)*: **FAIRCHILD SEMICONDUCTOR CORPORATION** [US/US]; 82 Running Hill Road, South Portland, ME 04106 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SHENOY, Praveen, Muraleedharan** [IN/US]; 18 B Wilkeswood Drive, Wilkes-Barre, PA 18702 (US).

(74) Agents: **REGAN, Christopher, F.** et al.; Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A., 255 South Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, FL 32802-3791 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

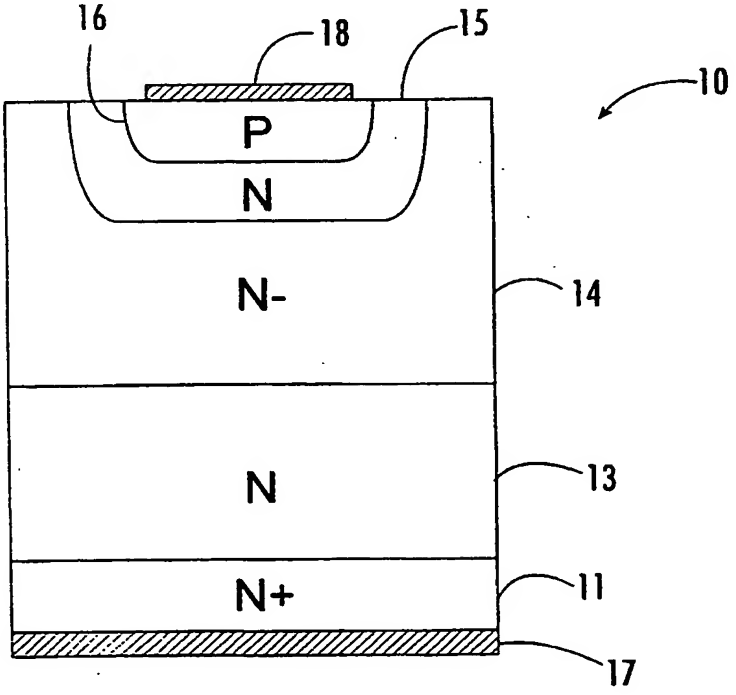
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
18 April 2002

[Continued on next page]

(54) Title: SOFT RECOVERY POWER DIODE AND RELATED METHOD



(57) Abstract: A semiconductor diode includes a first semiconductor layer including a dopant having a first conductivity type. A second semiconductor layer is adjacent the first semiconductor layer and includes a dopant having the first conductivity type and having a dopant concentration less than a dopant concentration of the first semiconductor layer. Adjacent the second semiconductor layer is a third semiconductor layer including a dopant having the first conductivity type and having a dopant concentration greater than the dopant concentration of the second semiconductor layer. A fourth semiconductor layer is adjacent the third semiconductor layer and includes a dopant of a second conductivity type. Respective contacts are connected to the first and fourth semiconductor layers.

WO 02/01643 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 01/19990

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/861

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 614 231 A (MITSUBISHI ELECTRIC CORP) 7 September 1994 (1994-09-07) figures 12A,12B	1-52
X	US 5 977 611 A (SITTIG ROLAND ET AL) 2 November 1999 (1999-11-02) figure 1	1-6, 8-21, 23-35, 37-52
X	US 4 228 453 A (PEARSALL THOMAS P) 14 October 1980 (1980-10-14) figure 2	1,16,31, 45

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2002	21/02/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

1

Form PCT/ISA/210 (second sheet) (July 1992)

BNSDOCID: <WO_____0201643A3_I_>

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19990

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BANERJEE J P ET AL: "DESIGN AND OPTIMIZATION OF THE DOPING PROFILE OF DOUBLE DRIFT LOW-HIGH-LOW INDIUM PHOSPHIDE DIODES" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 6, no. 7, 1 July 1991 (1991-07-01), pages 663-669, XP000227432 ISSN: 0268-1242 figure 1 ---	1,16,31, 45
X	US 5 032 540 A (FOLLEGOT JEAN-PIERRE) 16 July 1991 (1991-07-16) figure 8 ---	1,16,31, 45
A	EP 0 749 166 A (MITSUBISHI ELECTRIC CORP) 18 December 1996 (1996-12-18) figures 1-12,15-17 ---	12,27, 41,51
A	US 4 594 602 A (IIMURA KENJI ET AL) 10 June 1986 (1986-06-10) cited in the application figures 1A,1B -----	12,27, 41,51

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/19990

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0614231 A	07-09-1994	JP 6314801 A	08-11-1994
		EP 0614231 A2	07-09-1994
US 5977611 A	02-11-1999	DE 19713962 C1	02-07-1998
		EP 0869560 A2	07-10-1998
		JP 10284738 A	23-10-1998
US 4228453 A	14-10-1980	FR 2395605 A1	19-01-1979
		CA 1114521 A1	15-12-1981
		DE 2826999 A1	18-01-1979
		GB 1591000 A	10-06-1981
		JP 54008990 A	23-01-1979
US 5032540 A	16-07-1991	FR 2638892 A1	11-05-1990
		DE 68915510 D1	30-06-1994
		DE 68915510 T2	05-01-1995
		EP 0368768 A1	16-05-1990
		JP 2180015 A	12-07-1990
		JP 2697199 B2	14-01-1998
EP 0749166 A	18-12-1996	JP 8316500 A	29-11-1996
		DE 69609903 D1	28-09-2000
		DE 69609903 T2	29-03-2001
		EP 0749166 A1	18-12-1996
		US 5811873 A	22-09-1998
US 4594602 A	10-06-1986	JP 59189679 A	27-10-1984
		DE 3462642 D1	16-04-1987
		EP 0122598 A2	24-10-1984